

TEST REPORT IEC 62116 Test procedure of islanding prevention measures for utilityinterconnected photovoltaic inverters

Report Number	GZES191002576302
Date of issue	07/11/2019
Total number of pages	12
Name of Testing Laboratory preparing the Report:	SGS-CSTC Standards Technical Services Co., Ltd. Guangzhou Branch
Applicant's name:	EVOLVE ENERGY GROUP CO., LIMITED
Address:	RM 702, 7/F FU FAI COMM CTR 27 HILLIER ST SHEUNG WAN, HK
Test specification:	
Standard:	IEC/EN 62116: 2014 (Second Edition)
Test procedure:	Characteristic Examination
Non-standard test method:	N/A
Test Report Form No	IEC62116B
Test Report Form(s) Originator:	TÜV SÜD Product Service GmbH
Master TRF:	Dated 2014-10
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Test item description:	Solar Grid-tied Inverter
Trade Mark	EVIVO
Manufacturer:	EVOLVE ENERGY GROUP CO., LIMITED
Address:	RM 702, 7/F FU FAI COMM CTR 27 HILLIER ST SHEUNG WAN, HK
Model/Type reference .:	EVVO 3200TL-AV, EVVO 3000TL-AV, EVVO 2700TL-AV,
	EVVO 2200TL-AV, EVVO 1600TL-AV, EVVO 1100TL-AV
Ratings:	See model list in Page 6.
	Test Serial Number: SA3ES027K4P020
	Test Firmware version: V100

Respo	nsible Testing Laboratory (as applicable), testing procedure a	nd testing location(s):
⊟	CB Testing Laboratory:		
Testine	g location/ address:		
⊟	Associated CB Testing Laboratory:		
	Testing procedure: TMP/CTF Stage 1:	Shenzhen SOFAR SO	LAR Co., Ltd.
Testing	g location/ address:	XingDong Community,	ngDa Industrial Park, District 68, XinAn Street, BaoAn District, Joong Province, P.R. China
Tested	by (name, function 安NICES CQ_DD 安凡ICES CQ_DD (TATACH TATACH T	go zhang oject Engineer)	1dugo 2 hang
Approved by (name, funct 来 新 新		ger Hu echnical Reviewer)	Regula
	Testing procedure: WMT/CTF Stage 2:		
	Testing procedure: SMT/CTF Stage 3 or 4:		



	50) Hz	
Attachment #	Descri	ption	Pages
Attachment I	Pictures of the EUT and E	lectrical Schemes	12 pages
Attachment II	Graphics of the Test Resu		3 pages
Attachment III	Graphics of the Islanding	Behavior Detection	22 pages
Attachment IV	Testing Information		6 pages
Summary of testing:			
Tests performed (nam	ne of test and test	Testing location:	
clause):		Shenzhen SOFAR So	OLAR Co., Ltd.
 All clauses except: Sub-clause d) of the Table 5 of the point 6.1. Voltage and frequency trips shall be adjusted according to National Standards and/or local codes. From the result of inspection and tests performed 		(All clauses)	
on the submitted sar complies with the requi	nple we conclude that it rements of the Standard.		
below: - IEC/EN 62116:			
Summery of complian	ce with National Difference	S:	



Copy of marking plate(representative):

EVIVO	Solar Grid-tied Inverter
Model No:	EVVO 2700TL - AV
Max.DC Input Voltage	550V
Operating MPPT Voltag	ge Range 50~550V
Max. Input Current	12A
Max PV/Isc	15A
	L/N/PE, 230Vac
Max. Output Current	13A
Nominal Grid Freque	ncy <u>50/60Hz</u>
Max.OutputPower	
	1(adjustable+/-0.8)
Ingress Protection	
	re Range -30°C~+60°C
Desta ative Olana	Class I
	Non-Isolated
Factory - Shenzhen C	
	NE RGY G ROUP CO., LIMITED FAI COMM CTR 27 HILLIER ST e
VDE0126-1-1, VDE-AR-N4105, I IEC62116, UTE C15-712-1, AS47	
🗇 🛆 🗊	<u>AO. A X</u>

Note:

- 1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
- 2. Label is attached on the side surface of enclosure and visible after installation
- 3. Labels of other models are as the same with EVVO 2700TL-AV's except the parameters of rating.



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Test item particulars	Solar Grid-tied Inverter (Single Phase Inverter)
Classification of installation and use	Fixed (permanent connection)
Supply Connection	DC; PV
	AC; Grid connection
Possible test case verdicts:	
- test case does not apply to the test object	: N/A
- test object does meet the requirement	: P (Pass)
- test object does not meet the requirement	: F (Fail)
Testing	CTF Stage 1 procedure
Date of receipt of test item	: N/A
Date (s) of performance of tests	: From 11/06/2019

General remarks:

"(See Enclosure #)" refers to additional information appended to the report. "(See appended table)" refers to a table appended to the report.

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Throughout this report a \Box comma / \boxtimes point is used as the decimal separator.

Manufacturer's	s Declaration	per sub-clause	4.2.5	of IECEE 02:
manaotaror	5 Boolaration			

The application for obtaining a CB Test Certificate includes more than one factory location and a declaration from the Manufacturer stating that the sample(s) submitted for evaluation is (are) representative of the products from each factory has been provided	 ☐ Yes ☑ Not applicable
When differences evict, they shall be identified in the	• O a manual manual information as ation

When differences exist; they shall be identified in the General product information section.

 Name and address of factory (ies)
 Dongguan SOFAR SOLAR Co.,Ltd.

 1F - 6F, Building E, No. 1 JinQi Road, Bihu
 Industrial Park, Wulian Village, Fenggang Town,

 Dongguan City,Guangdong Province,P.R. China.



General product information:

Product covered by this report is grid-connected PV inverter for indoor or outdoor installation. The connection to the DC input and AC output are through connectors.

The Solar inverter converts DC voltage into AC voltage.

The input and output are protected by varistors to Earth. The unit is providing EMC filtering at the output toward mains. The unit does not provide galvanic separation from input to output (transformerless). The output is switched off redundant by the high power switching bridge and a two relays. This assures that the opening of the output circuit can operate in case of one error.

Equipment Under Testing:

– EVVO 2700TL-AV

Variant models:

- EVVO 3200TL-AV
- EVVO 3000TL-AV
- EVVO 2200TL-AV
- EVVO 1600TL-AV
- EVVO 1100TL-AV

Model Number	EVVO	EVVO	EVVO	EVVO	EVVO	EVVO
	3200TL-AV	3000TL-AV	2700TL-AV	2200TL-AV	1600TL-AV	1100TL-AV
Max. input voltage		550Vd.c.		500Vd.c		
Max. input current	12Ad.c.	12Ad.c.	12Ad.c.	12Ad.c.	12Ad.c.	12Ad.c.
Operating MPPT voltage range		50-550Vd.c.			50-500Vd.c.	
Full load DC Voltage	300-500	275-500	250-500	200-450	150-450	110-450
Range	Vd.c.	Vd.c.	Vd.c.	Vd.c.	Vd.c.	Vd.c.
Rated voltage	360V					
Rated grid voltage	230Va.c.					
Rated grid frequency		50Hz				
Rated output power	3.3kW	3.0kW	2.7kW	2.2kW	1.6kW	1.1kW
Rated output current	13Aa.c.	13 Aa.c.	11.8Aa.c.	9.6Aa.c.	7Aa.c.	4.8Aa.c.
Max. Output Current	16Aa.c.	14.5 Aa.c.	13Aa.c.	10.6Aa.c.	7.7Aa.c.	5.3Aa.c.
Power factor	0.8 leading to 0.8 lagging					
Ambient temperature	-30 °C ~60°C					
Ingress protection	IP65					
Protective class	Class I					

The variants models have been included in this test report without tests because the following features don't change regarding to the tested model:

- Same connection system and hardware topology
- Same control algorithm.
- Output power within 2,5 and 2/3 of the EUT or Modular inverters.
- Same Firmware Version



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Clause Req

Requirement + Test

Result - Remark

Verdict

4	Testing circuit		
	The testing circuit shown in Figure 1 is employed.		Р
	Similar circuits are used for three-phase output.		Р
	Parameters to be measured are shown in Table 1		Р
	and Figure 1. Parameters to be recorded in the test		
	report are discussed in Clause 7.		
5	Testing equipment		
5.1	Measuring instruments		Р
	islanding test until the EUT ceases to energize the me island.	nalyzer equipped with emory function aveform caught from the	Ρ
		vitch open and the EUT ease to energize	
	For multi-phase EUT, all phases are monitored.		Р
	A waveform monitor designed to detect and Sec	ee Annex IV for testing guipment information	P
	For multi-phase EUT, the test and measurement equipment is recorded each phase current and each phase-to-neutral or phase-to-phase voltage, as appropriate, to determine fundamental frequency active and reactive power flow over the duration of the test.	· · ·	Р
		ess than 1% of the rated JT output current	Р
	Current, active power, and reactive power measurements through switch S1 used to determine the circuit balance conditions report the fundamental (50 Hz or 60 Hz) component.		Ρ
5.2	DC power source		
5.2.1	General		Р
	A PV array or PV array simulator (preferred) may be Ch used. If the EUT can operate in utility-interconnected mode from a storage battery, a DC power source may be used in lieu of a battery as long as the DC power source is not the limiting device as far as the maximum EUT input current is concerned.	nroma PV simulator used	Ρ
	The DC power source provides voltage and current necessary to meet the testing requirements described in Clause 6.		Ρ
5.2.2	PV array simulator		Р
	The tests are conducted at the input voltage defined in Table 2 below, and the current is limited to 1,5 times the rated photovoltaic input current, except when specified otherwise by the test requirements.		P
	A PV array simulator is recommended, however, any type of power source may be used if it does not influence the test results.		Р
5.2.3	Current and voltage limited DC power supply with series resistance		N/A



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Clause Requirement + Test

Result - Remark

Verdict

5.4	AC loads					
	1) Three-phase case only					
	Phase angle distance 1) 120 ° ± 1,5 °					
	Frequency Nominal ±0,1 Hz Phase angle distance 1) 120 % ± 1.5 %					
	Voltage THD < 2,5 %					
	Voltage Nominal ±2,0 %					
	Items	Conditions Section 4				
	Table 4 – AC power source requirem					
	Table 4.					
	· · · · · · · · · · · · · · · · ·	ions specified in the conditions specified				
		source may be AC power source used meets	Р			
5.3	AC power source					
	array configuration to achieve the input voltage and power levels prescribed in 6.1.					
	reference device. It may be necess					
	measured by a silicon-type					
	by no more than 2 % over the durat		1 4/7 1			
	Testing is limited to times when the		N/A			
	maximum EUT input operating volta					
	of EUT maximum input power a		,//			
	A PV array used as the EUT input s	ource is capable	N/A			
5.2.4	PV array		N/A			
	Power factor: 0.25 to 0.8					
	allowable run-on time is exceeded.					
	achieved until the island condition					
	of the test: from the point where					
	within 2 % of specified power level over the duration					
	EUT MPPT, simulator output power remains stable					
	Stability: Excluding the variations caused by the					
	within 10% of its final value in less than 1ms.					
	change, results in a settling of the output current to					
	to a step in output voltage, due to a 5% load					
	Response speed: The response time of a simulator					
	output power and other levels specified by test conditions of table 5.					
	Output power: Sufficient to provide	maximum FLIT				
	the range:					
	resistance) is selected to provide a					
	A series resistance (and, optic		N/A			
	the series and shunt resistance des					
	current and open circuit voltage whe					
	voltage limit, set to provide the des		IN/A			
	The power source provides adjust		N/A			
	achieve EUT maximum output pov and maximum EUT input operating					
	capable of EUT maximum input					
	A DC power source used as the EL		N/A			



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	On the AC side of the EUT, variable resistance,	Passive loads (variable	P
	capacitance, and inductance are connected in	resistance, capacitance and	
	parallel as loads between the EUT and the AC	inductance) have been	
	power source. Other sources of load, such as	connected.	
	electronic loads, may be used if it can be shown that		
	the source does not cause results that are different		
	than would be obtained with passive resistors,		
	inductors, and capacitors.		
	All AC loads are rated for and adjustable to all test		Р
	conditions. The equations for Qf are based upon an		
	ideal parallel RLC circuit. For this reason, non-		
	inductive resistors, low loss (high Qf) inductors,		
	and capacitors with low effective series resistance		
	and effective series inductance are utilized in the		
	test circuit. Iron core inductors, if used, are not		
	exceed a current THD of 2 % when operated at		
	nominal voltage. Load components are		
	conservatively rated for the voltage and power levels		
	expected. Resistor power ratings are chosen so as		
	to minimize thermally-induced drift in esistance		
ļ	values during the course of the test.		
	Active and reactive power is calculated (using the		P
	measurements provided in Table 1) in each of the R,		
	L and C legs of the load so that these parasitic		
	parameters (and parasitics introduced by variacs or		
	autotransformers) are properly accounted for when		
	calculating Qf.		
6	Test for single or multi-phase inverter		
6.1	Test procedure	(see appended table)	P
	The test uses an RLC load, resonant at the EUT		P
	nominal frequency (50 Hz or 60 Hz) and matched to		
	the EUT output power.		
			P
	the EUT output power.		Р
	the EUT output power. For multi-phase EUT, the load is balanced across all		Р
	the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all		P
	the EUT output power.For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phasesThis test is performed with the EUT conditions as in		
	the EUT output power.For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phasesThis test is performed with the EUT conditions as in Table 5, where power and voltage values are given		
	the EUT output power.For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phasesThis test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating.		
	the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power		P
	the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b).Adjusting the DC input source		P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 		P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) .Adjusting the DC input source c)Turn off the EUT and open S1 d) .Adjust the RLC circuit to have Qf = 1.0 ±0.05 		P P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to 		P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b).Adjusting the DC input source c)Turn off the EUT and open S1 d).Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to the EUT by closing S2 		P P P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to the EUT by closing S2 f)Open the utility-disconnect switch S1 to initiate 		P P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to the EUT by closing S2 f)Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. 		P P P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to the EUT by closing S2 f)Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g)For test condition A, adjust the real load and only 		P P P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to the EUT by closing S2 f)Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g)For test condition A, adjust the real load and only one of the reactive load components to each of 		P P P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to the EUT by closing S2 f)Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g)For test condition A, adjust the real load and only one of the reactive load components to each of the load imbalance conditions shown in the 		P P P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to the EUT by closing S2 f)Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g)For test condition A, adjust the real load and only one of the reactive load components to each of the load imbalance conditions shown in the shaded portion of table 6. If any of the recorded 		P P P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to the EUT by closing S2 f)Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g)For test condition A, adjust the real load and only one of the reactive load components to each of the load imbalance conditions shown in the shaded portion of table 6. If any of the recorded run-on times are longer than the one recorded for 		P P P P P P
	 the EUT output power. For multi-phase EUT, the load is balanced across all phases and the switch S1 as in Figure 1 opens all phases This test is performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating. a)Determine EUT test output power b) Adjusting the DC input source c)Turn off the EUT and open S1 d) Adjust the RLC circuit to have Qf = 1.0 ±0.05 e)Connect the RLC load configured in step d) to the EUT by closing S2 f)Open the utility-disconnect switch S1 to initiate the test, Run-on time is recorded. g)For test condition A, adjust the real load and only one of the reactive load components to each of the load imbalance conditions shown in the shaded portion of table 6. If any of the recorded 		P P P P P P



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			1	

			_
	h) For test condition B and C, adjust the only one		Р
	reactive load components by approximately 1,0%		
	per test, within a total range of 95% to 105% of the		
	operating point. If run-on times are still increasing at		
	the 95% or 105% points, additional 1% increments		
	have to be taken until run-on times begin		
	decreasing.		
6.2	Pass/fail criteria		
	An EUT is considered to comply with the	Run-on time is less than 2s in	Р
	requirements for islanding protection when each	any case	
	case of recorded run-on time is less than 2 s or		
	meets the requirements of local codes.		
7	Documentation		
	At a minimum, the following information is recorded		Р
	and maintained in the test report.		
	a) Specifications of EUT. Table 8 provides an		Р
	example of the type of information that is provided.		
	b) Measurement results. Table 9 provides an		Р
	example of the type of information that is provided.		
	Actual measured values is to be recorded.		
	c) Block diagram of test circuit.		Р
	d) Specifications of the test and measurement		Р
	equipment. Table 10 provides an example of the		
	type of information that is provided.		
	e) Any test configuration or procedure details such		Р
	as methods of achieving specified load and EUT		
	output conditions.		
	f) Any additional information required by the testing		Р
	laboratory's accreditation.		
	g) Specify the evaluation criterion from clause 6.2		Р
	that was utilized to determine if the product passed		
	or failed the test.		
Annex A	Islanding as it applies to PV systems(Informative)		
A.1	General		
A.2	Impact of distortion on islanding		
Annex B	Test for independent islanding detection device (relay	/)(Informative)	
B.1	Introduction		
B.2	Testing circuit		
B.3	Testing equipment		
B.4	Testing procedure		
B.5	Documentation		



6.1	Table: tested condition and run-on time						Р		
No.	P _{EUT} (% of EUT rating)	Reactiv e load (% of normial)	Pac	Qac	Run-on time(ms)	Peut (W)	Actual Q _f	V _{DC} (d.c.V)	Which load is selected to be adjusted (R or L)
	1	1		Test co	ondtion A			1	1
1	100	100	0	0	408	2698	1.00	464.9	
2	100	100	-5	-5	324	2701	1.05	465.9	R/L
3	100	100	-5	0	364	2700	1.05	465.9	R
4	100	100	-5	+5	320	2701	1.02	466.1	R/L
5	100	100	0	-5	284	2698	1.03	465.0	L
6	100	100	0	+5	322	2689	0.98	460.3	L
7	100	100	+5	-5	318	2689	0.98	460.0	R/L
8	100	100	+5	0	332	2675	0.96	455.3	R
9	100	100	+5	+5	288	2696	0.95	462.9	R/L
10	100	100	-10	+10					R/L
11	100	100	-5	+10					R/L
12	100	100	0	+10					L
13	100	100	+10	+10					R/L
14	100	100	+10	+5					R/L
15	100	100	+10	0					R
16	100	100	+10	-5					R/L
17	100	100	+10	-10					R/L
18	100	100	+5	-10					R/L
19	100	100	+5	10					R/L
20	100	100	0	-10					L
21	100	100	-5	-10					R/L
22	100	100	-10	-10					R/L
23	100	100	-10	-5					R/L
24	100	100	-10	0					R/L
25	100	100	-10	+5					R/L
Test condtion B									



10	66	66	0	0	434	299.6	1.00	1783	
11	66	66	0	-5	292	299.5	1.02	1783	L
12	66	66	0	-4	352	299.4	1.02	1782	L
13	66	66	0	-3	338	298.1	1.01	1782	L
14	66	66	0	-2	340	298.6	1.01	1783	L
15	66	66	0	-1	308	299.6	1.00	1782	L
16	66	66	0	1	352	300.1	1.00	1782	L
17	66	66	0	2	344	298.9	0.99	1782	L
18	66	66	0	3	312	299.8	0.99	1783	L
19	66	66	0	4	360	298.0	0.99	1781	L
20	66	66	0	5	314	297.6	0.98	1780	L
21	66	66	0	6					L
	•		•	Test co	ndition C		•		
22	33	33	0	0	332	143.9	1.00	904	
24	33	33	0	-5	264	143.6	1.03	897	L
25	33	33	0	-4	318	144.1	1.02	897	L
26	33	33	0	-3	330	143.9	1.01	897	L
27	33	33	0	-2	316	144.2	1.01	899	L
28	33	33	0	-1	326	145.2	1.01	899	L
29	33	33	0	1	314	143.0	1.00	900	L
30	33	33	0	2	312	144.9	0.99	903	L
31	33	33	0	3	300	143.3	0.99	901	L
32	33	33	0	4	286	144.2	0.98	903	L
33	33	33	0	5	142	143.6	0.97	900	L
34	33	33	0	6					L

Remark:

For test condition A:

If any of the recorded run-on times are longer than the one recorded for the rated balance condition, then the non-shaded parameter combinations also require testing.

For test condition B and C:

If run-on times are still increasing at the 95 % or 105 % points, additional 1 % increments is taken until run-on times begin decreasing.

--- End of test report---



IEC 62116:2014 (50Hz)

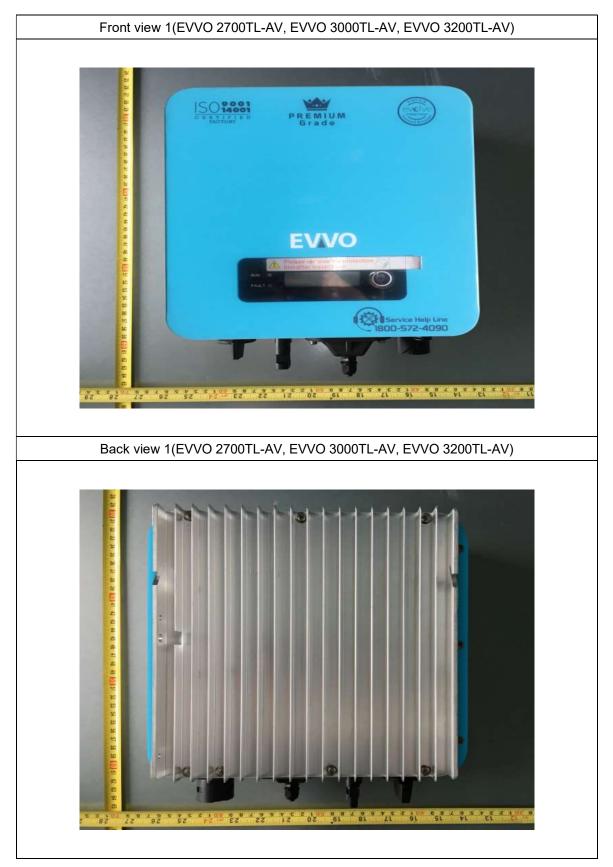
ATTACHMENT I

(Pictures of the EUT and Electrical Schemes)



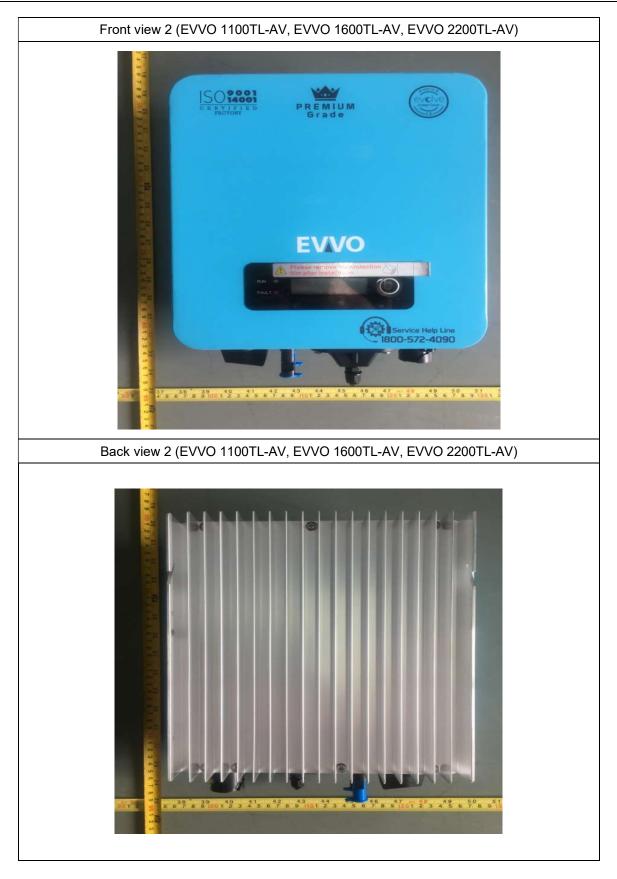
IEC 62116:2014 (50Hz)

1 PICTURES





Report Nº GZES191002576302



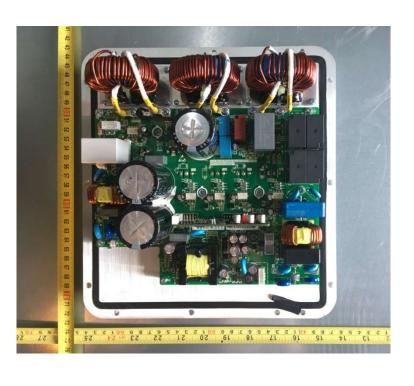


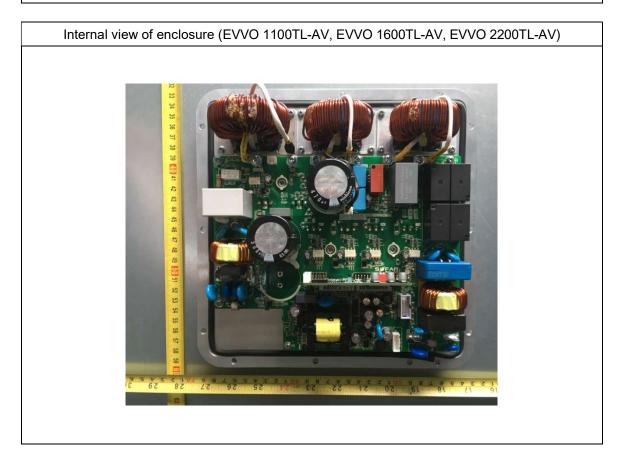
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IEC 62116:2014 (50Hz)

Internal view of enclosure (EVVO 2700TL-AV, EVVO 3000TL-AV, EVVO 3200TL-AV)

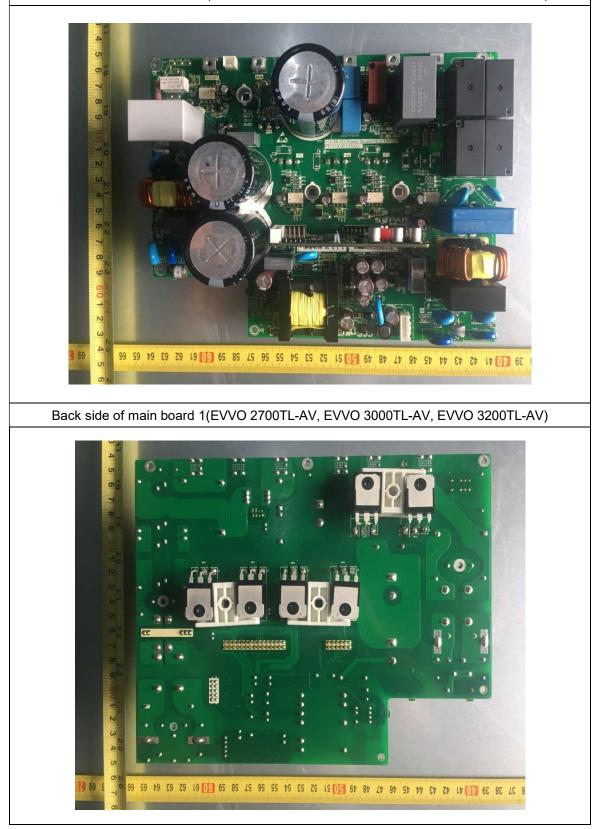






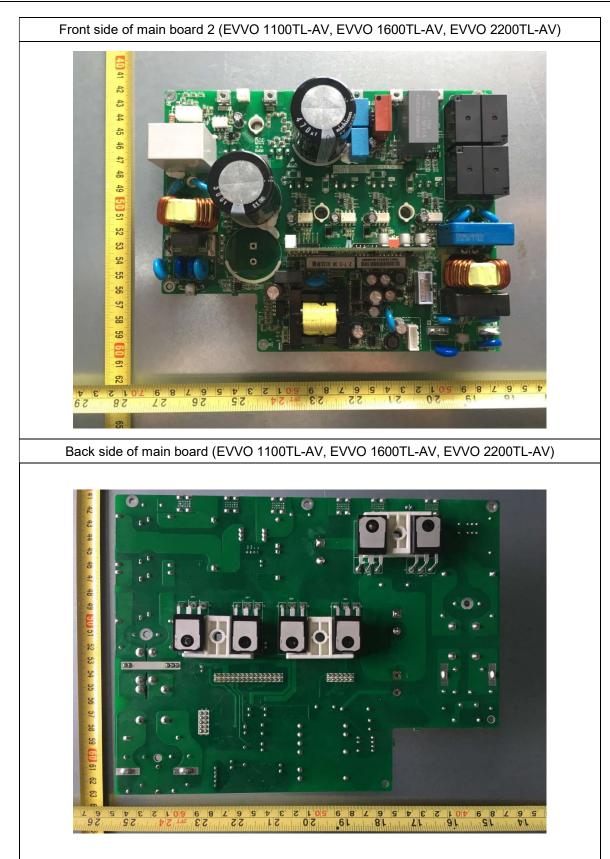
IEC 62116:2014 (50Hz)

Front side of main board 1(EVVO 2700TL-AV, EVVO 3000TL-AV, EVVO 3200TL-AV)



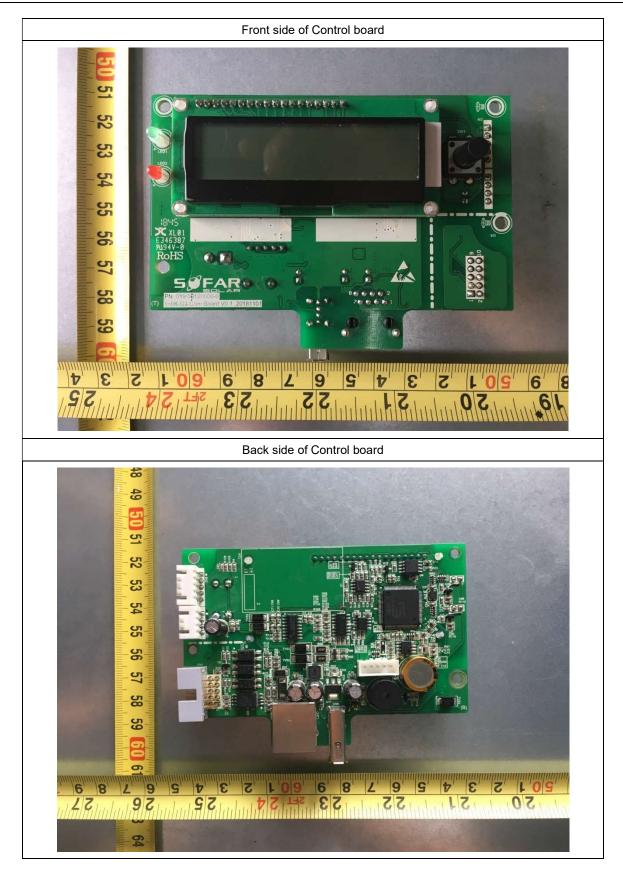


Report Nº GZES191002576302



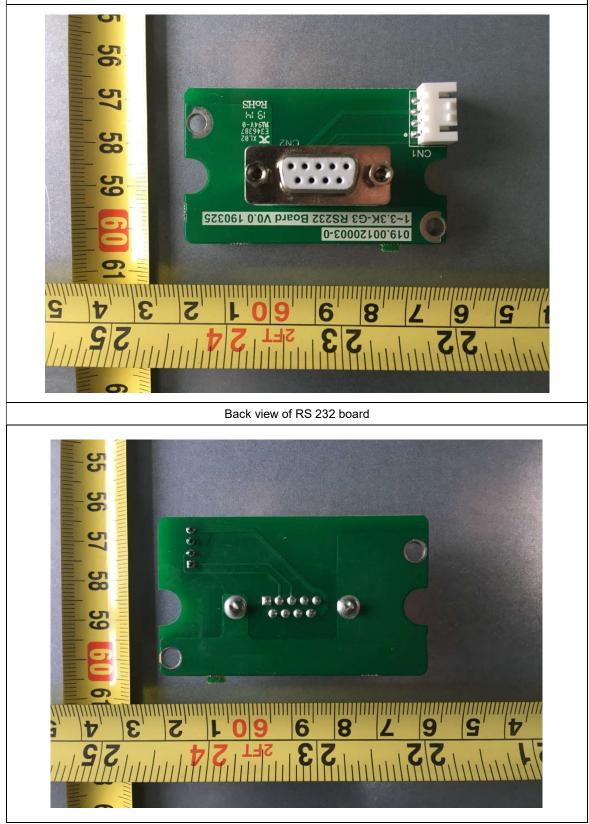


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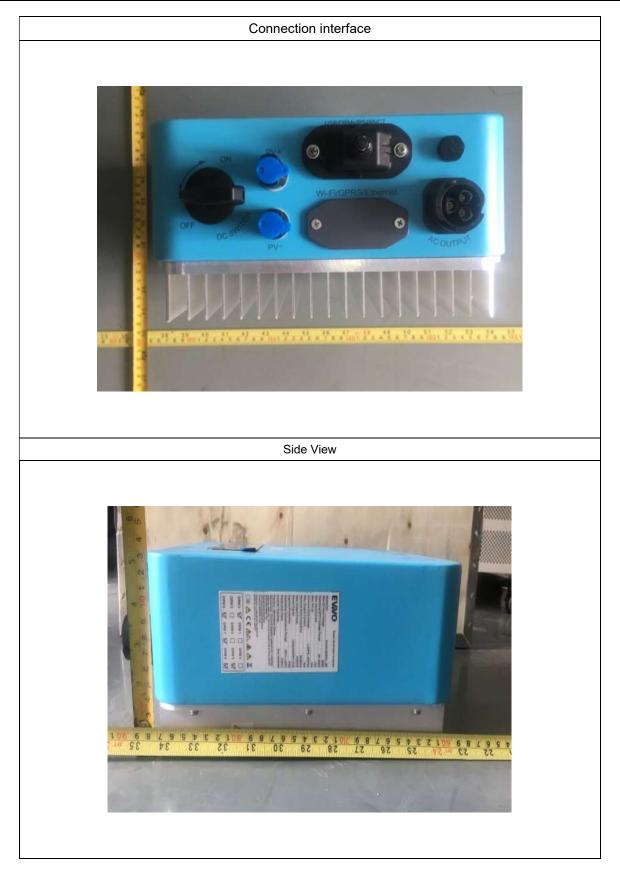




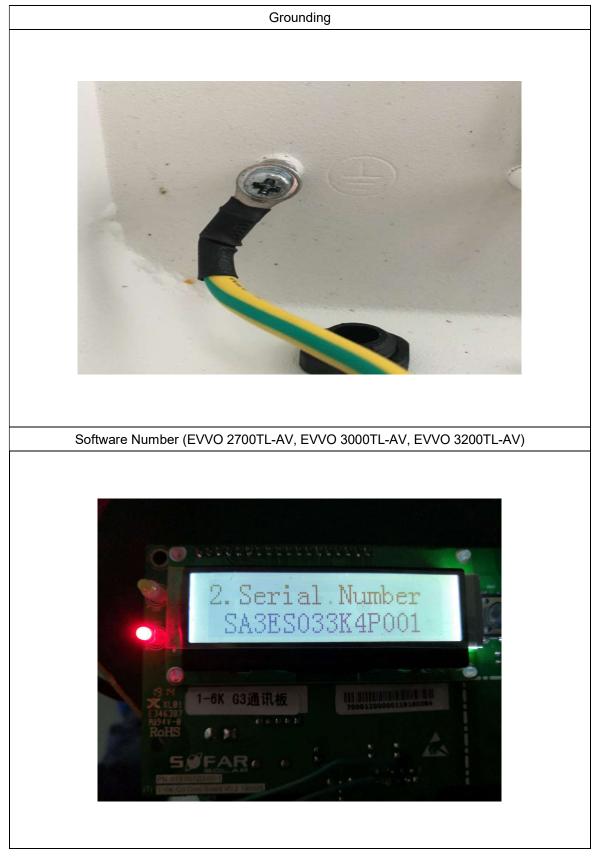




Report Nº GZES191002576302







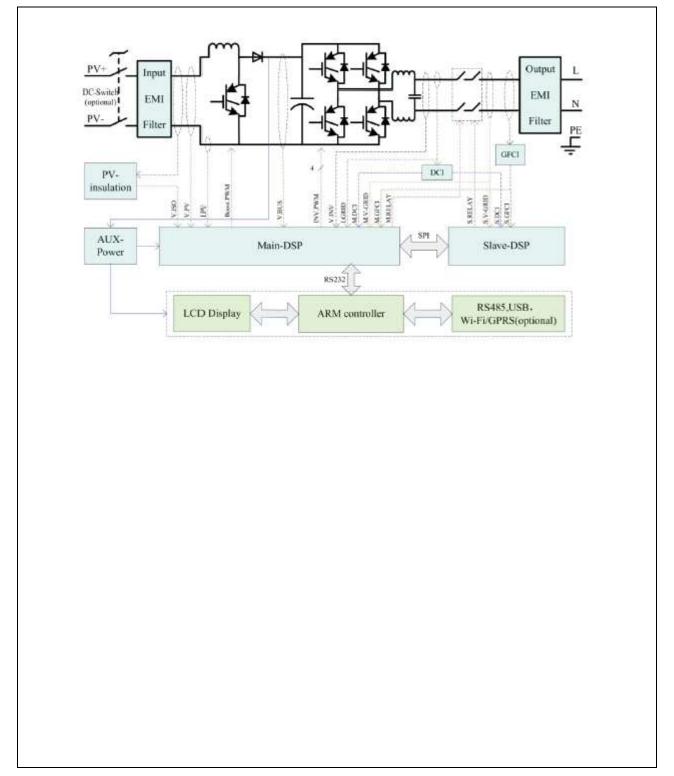






IEC 62116:2014 (50Hz)

Electrical Schemes





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IEC 62116:2014 (50Hz)

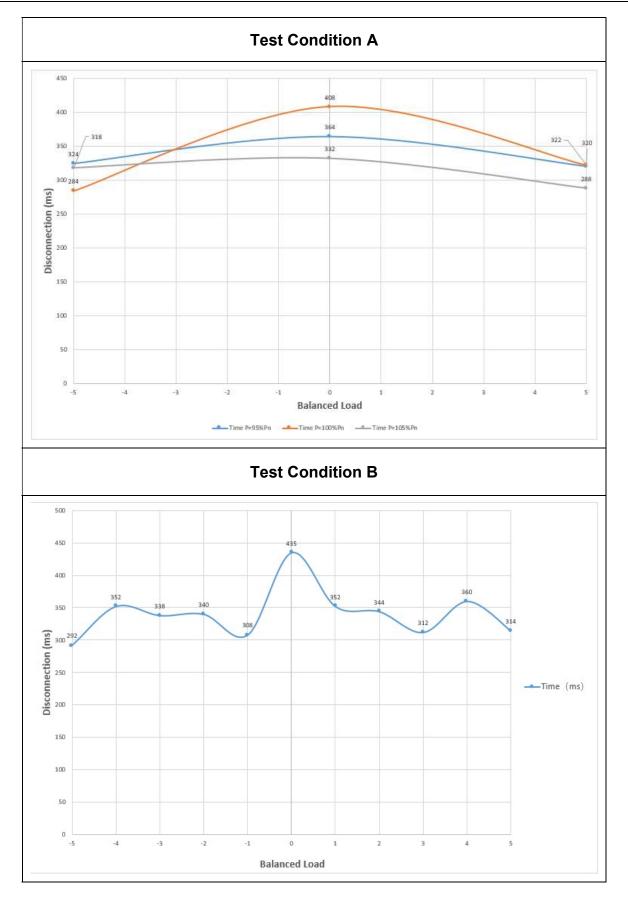
ATTACHMENT II

(GRAPHICS OF THE TEST RESULTS)



Report Nº GZES191002576302







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IEC 62116:2014 (50Hz)



Test Condition C 650.0 550.0 450.0 Disconnection (ms) 332 331 330 326 318 316 314 312 300 286 2 ----Time (ms) 150.0 50.0 -50.0 -4 -3 -2 2 3 4 5 -1 0 1 -5 **Balanced Load**



IEC 62116:2014 (50Hz)

ATTACHMENT III

(GRAPHICS OF THE ISLANDING BEHAVIOR DETECTION)



IEC 62116:2014 (50Hz)

1 DEFINITIONS

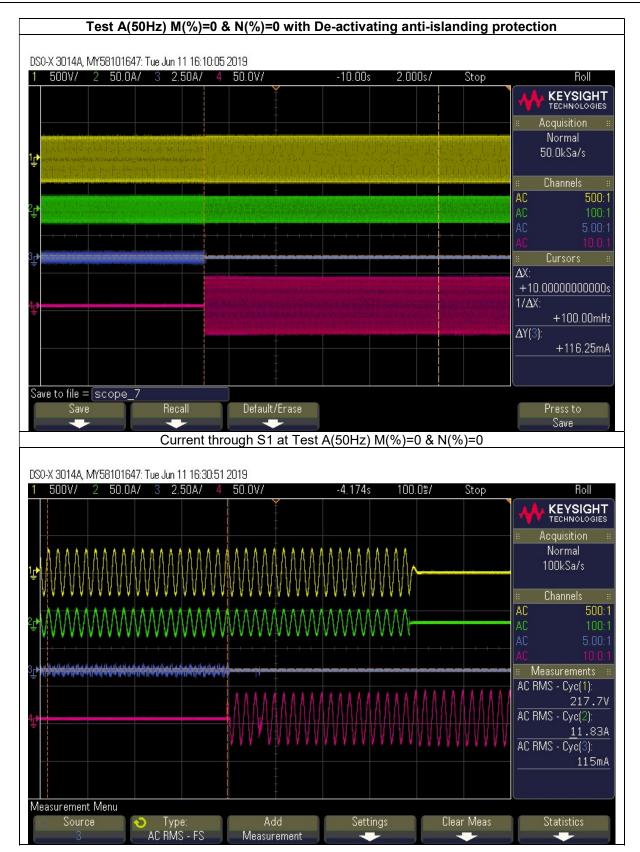
- M It represents the % change in active load from nominal output power
- N It represents the % change in reactive load from nominal output power

2 LEGEND

Legend					
DSO-X 3014A, MY58101647: Tue Jun 11 16: 1 500V/ 2 50.0A/ 3 2.50A/		IO.O [®] / Stop Roll KEYSIGHT TECHNOLOGIES Acquisition # Normal 100kSa/s			
		III Channels III AC 500:1 AC 100:1 AC 5.00:1 AC 100:1 AC 10.0:1 III Cursors ΔX: +408.000000000ms 1/ΔX: 1/ΔX:			
€ Cursors Menu ○ Mode ○ Source Manual 3	Cursors X2	X1: -4.278000000000s Y1: -112.75mA X2: -3.87000000000s Y1: -12.75mA			
Colour	Label CH1	Definition Output Voltage			
	CH2 CH4	Output Current Grid Switch			

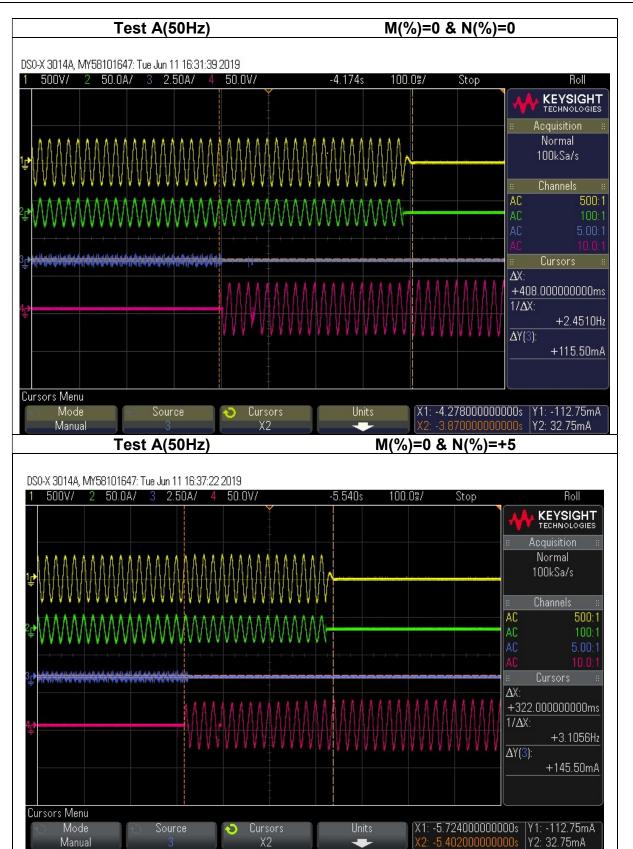


Report Nº GZES191002576302



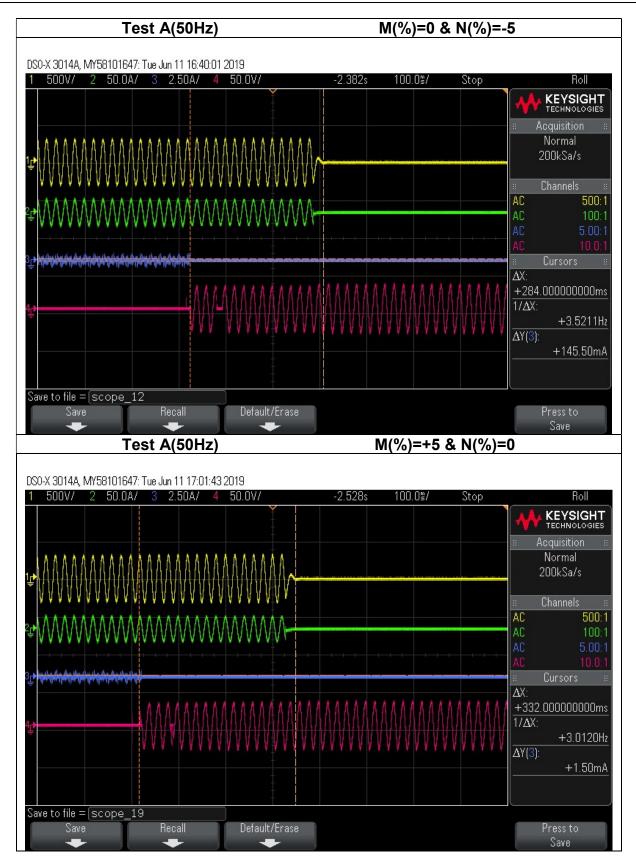


Report Nº GZES191002576302





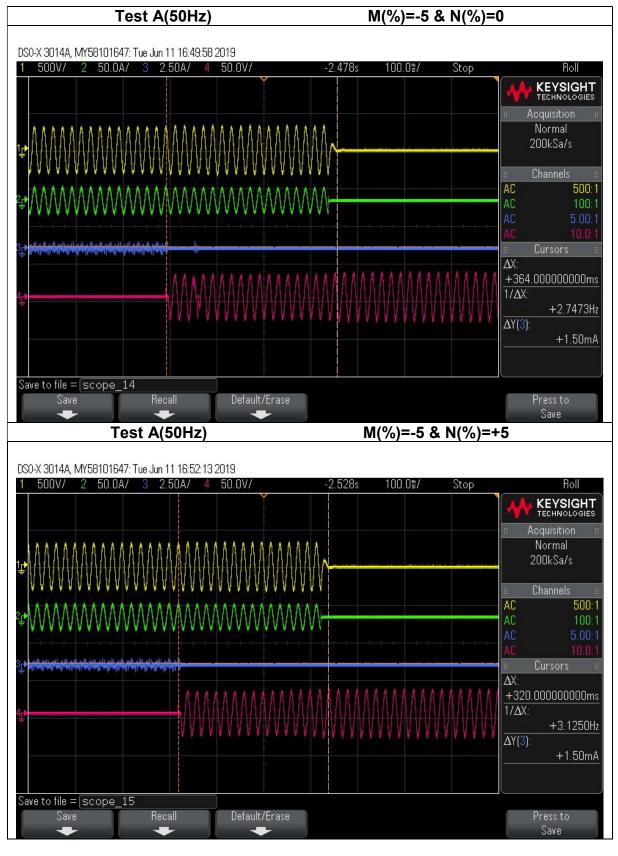
Report Nº GZES191002576302





Report Nº GZES191002576302

IEC 62116:2014 (50Hz)

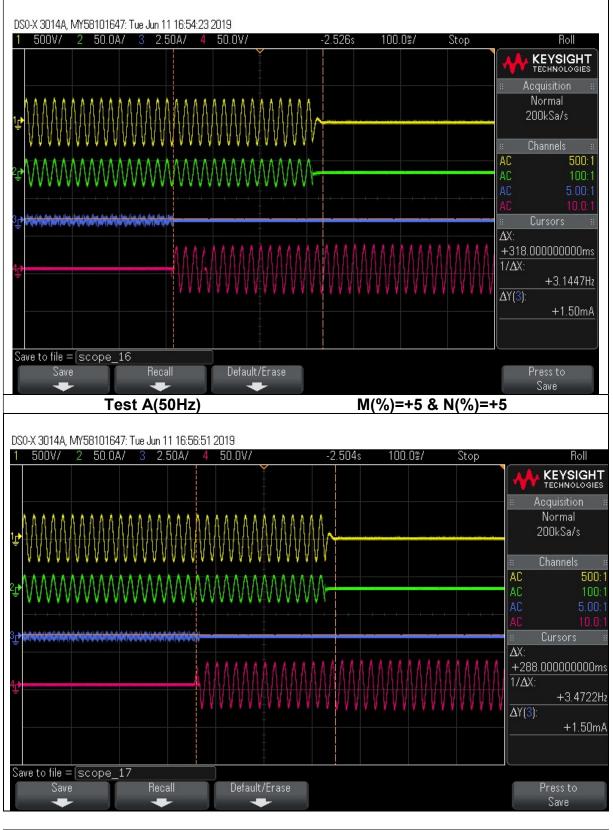


Test A(50Hz)

M(%)=+5 & N(%)=-5



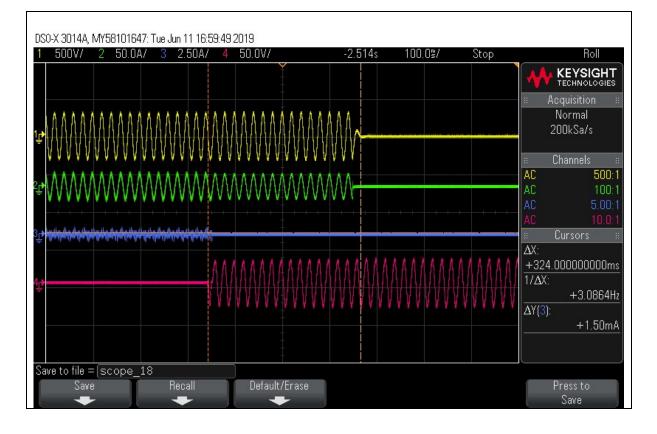
IEC 62116:2014 (50Hz)



Test A(50Hz)

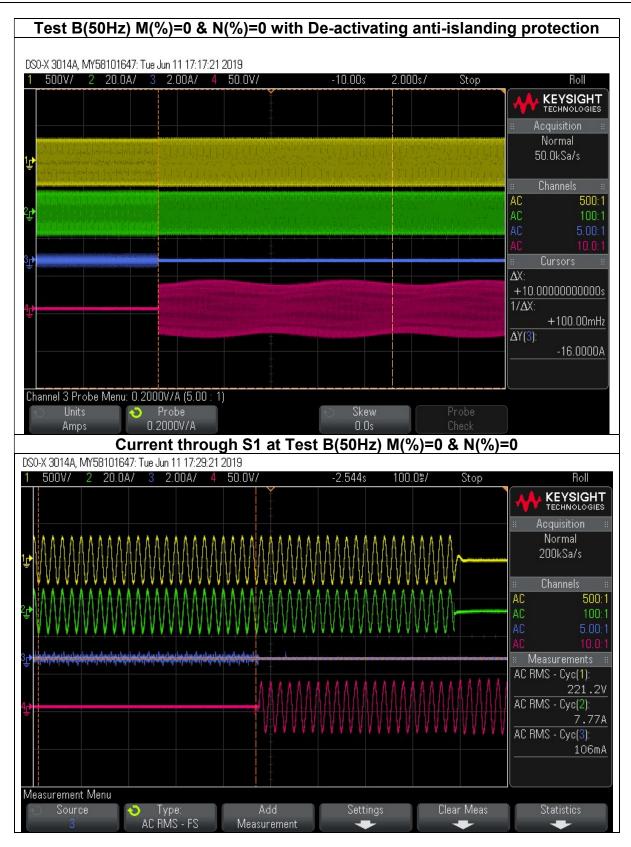
M(%)=-5 & N(%)=-5







Report Nº GZES191002576302





Report Nº GZES191002576302





ATTACHMENT III Report N° GZES191002576302

IEC 62116:2014 (50Hz)



Test B(50Hz)

M(%)=0 & N(%)=+4



ATTACHMENT III Report N° GZES191002576302

IEC 62116:2014 (50Hz)



Test B(50Hz)

M(%)=0 & N(%)=-1



ATTACHMENT III Report N° GZES191002576302

IEC 62116:2014 (50Hz)

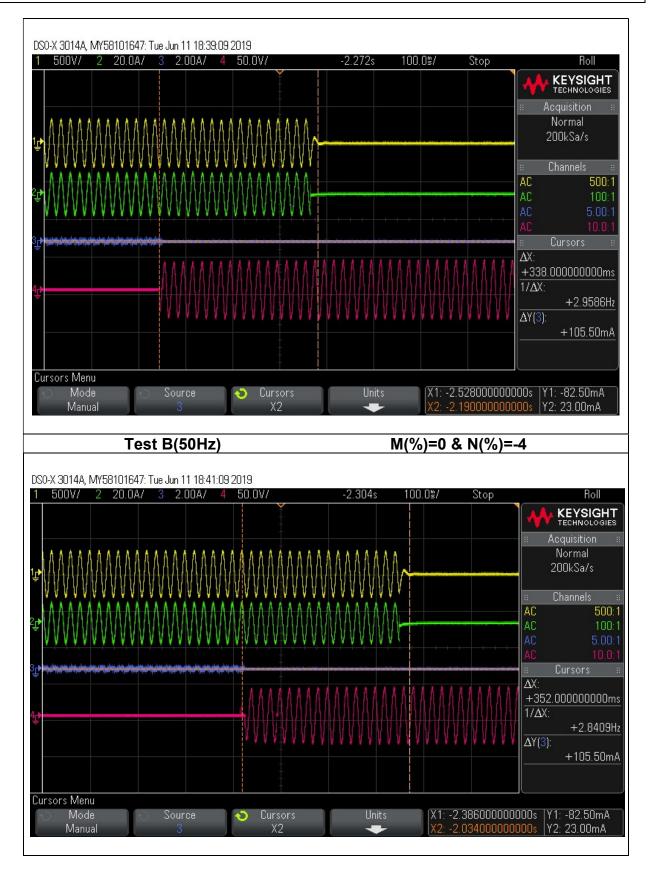


Test B(50Hz)

M(%)=0 & N(%)=-3

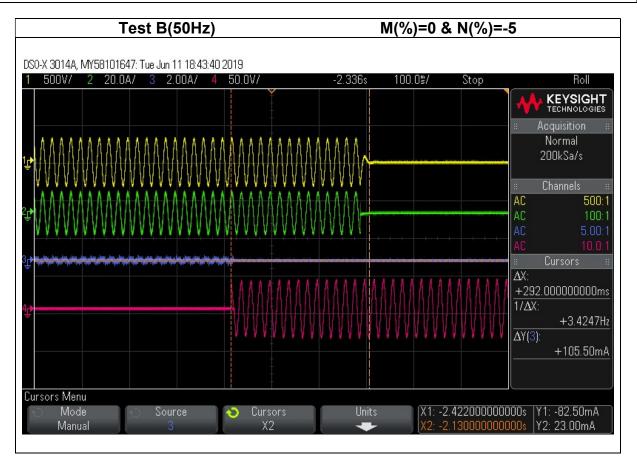


ATTACHMENT III Report Nº GZES191002576302



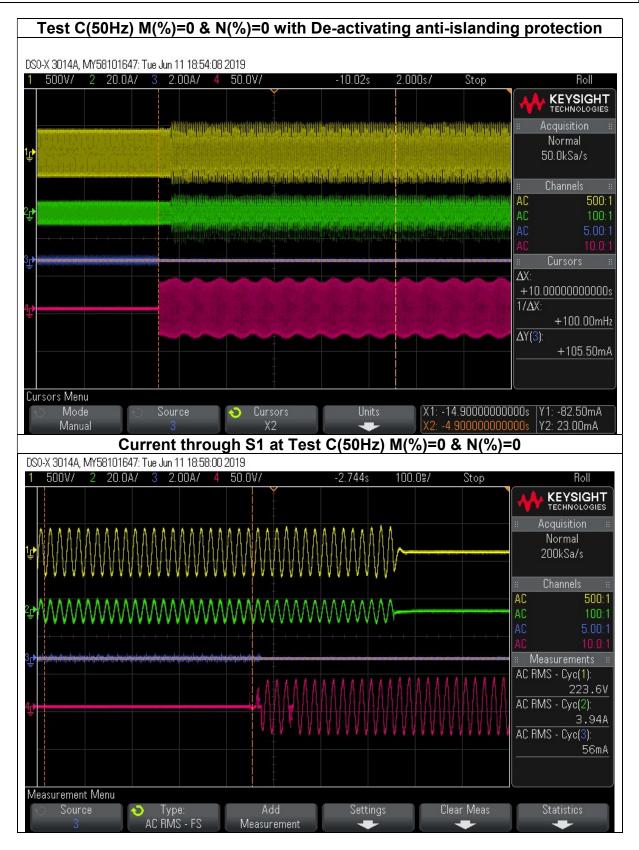


Report Nº GZES191002576302



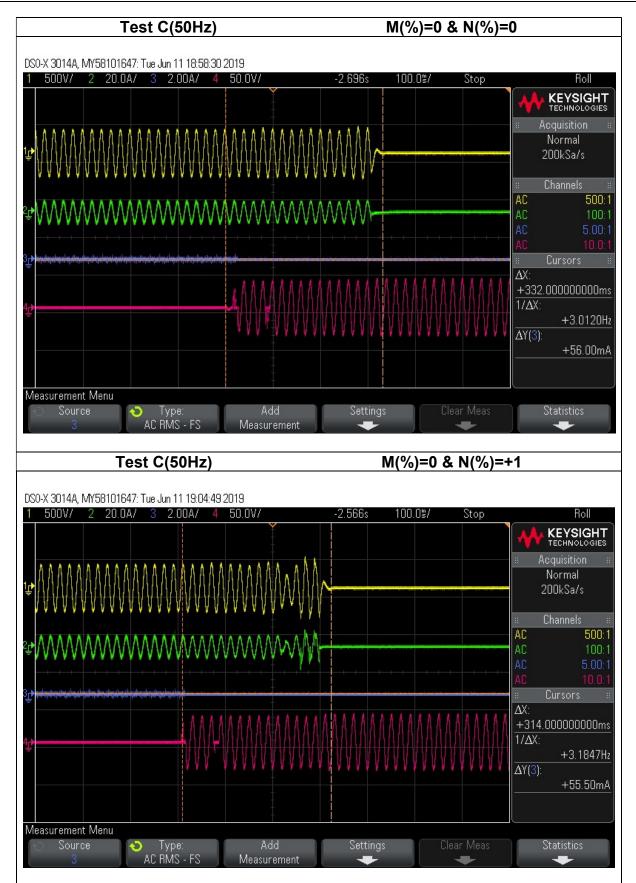


Report Nº GZES191002576302



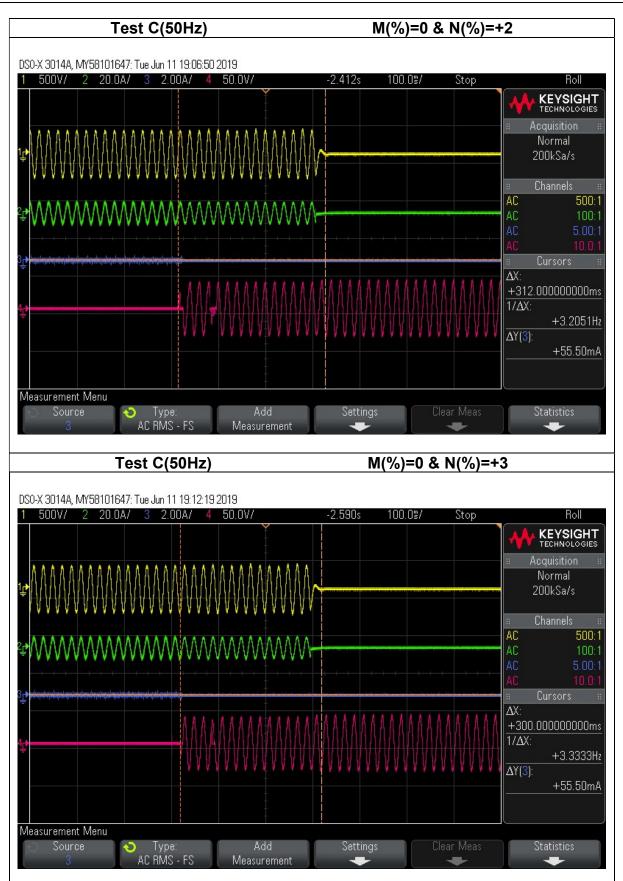


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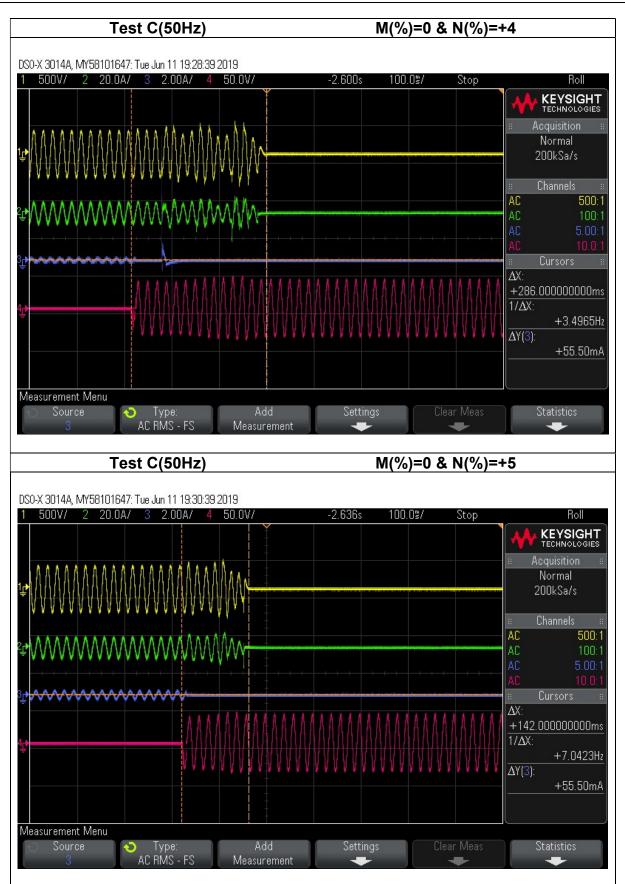


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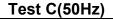
Report Nº GZES191002576302





Report Nº GZES191002576302

IEC 62116:2014 (50Hz)

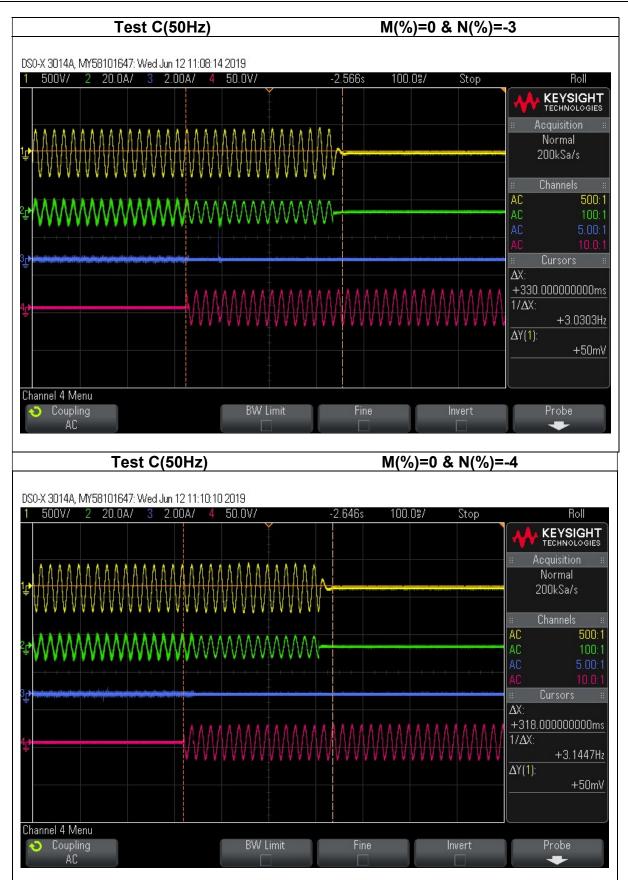


M(%)=0 & N(%)=-1



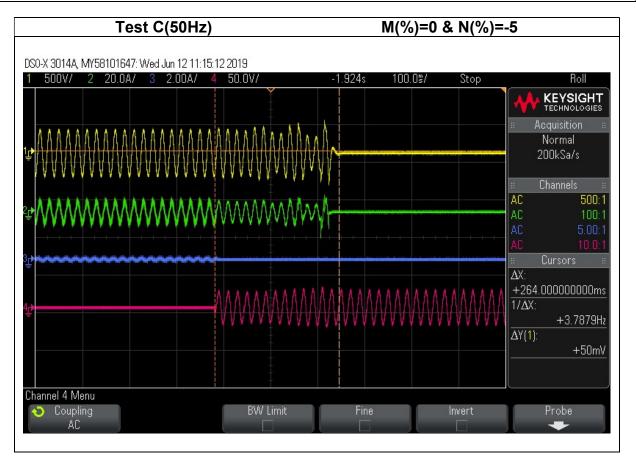


Report Nº GZES191002576302





Report Nº GZES191002576302





IEC 62116:2014 (50Hz)

ATTACHMENT IV

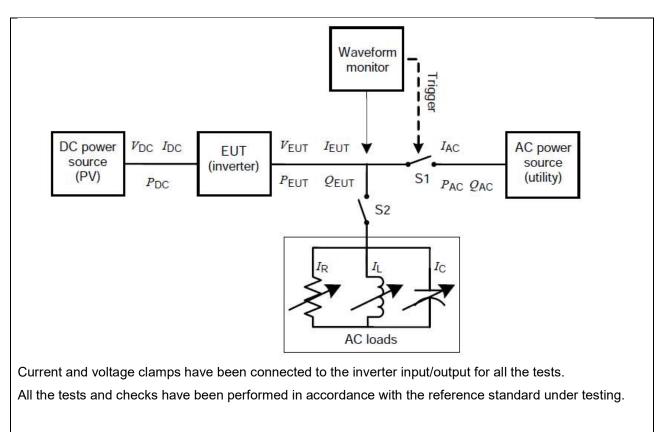
(Testing information)



Report Nº GZES191002576302

IEC 62116:2014 (50Hz)

1 TESTING CIRCUIT





Report Nº GZES191002576302

IEC 62116:2014 (50Hz)

2 TESTING EQUIPMENT

Fro m	No.	Equipment Name	Model No.	Equipment No.	Calibration Date	Equipment calibration due date	
	1	Digital oscilloscope	DS05014A	MY5007026 6	2019-02-13	2020-02-12	
	2	Voltage probe	SI-9110	111541	2019-02-13	2020-02-12	
	3	Voltage probe	SI-9110	152627	2019-02-13	2020-02-12	
	4	Voltage probe	SI-9110	111134	2019-02-13	2020-02-12	
lar	5	Power analyzer	WT3000	91N610888	2019-02-13	2020-02-12	
Sofarsolar	6	Current probe	i1000s	29503223	2019-02-13	2020-02-12	
So	7	Current probe	i1000s	30413448	2019-02-13	2020-02-12	
	8	Current probe	CP5150	C15015000 8	2019-02-13	2020-02-12	
	9	Temperature & Humidity meter	TH101B	201030245 220	2019-02-13	2020-02-12	
	10	Temperature & Humidity Chamber	HGTP-225R	HG1303080 1	2019-02-13	2020-02-12	
SGS	11	True RMS Multimeter	Fluke / 289C	GZE012-53	2019-02-26	2020-02-25	



Report Nº GZES191002576302

Items	Specifications				
1) PV array simulator					
a) Voltage range	0 – 1000Vdc (0.01V step)				
b) Current range	0 – 40A (0.01A step)				
2) AC power source	'				
a) Output wiring	Three phase				
b) Output capacity	100KVA				
c) Output voltage	10-300Vrms				
d) Output frequency	45-65Hz				
e) Voltage stability	<u>+</u> 100ppm/℃				
f) Output voltage distortion	0.05% max.				
3) Digital meter					
a) Voltage range	0 – 1000Vdc, 0 – 600Vrms				
b) Current range	0 – 30A				
c) Frequency range (accuracy)	0.2%				
d) Measurement items	Voltage (V) Current (A) Active power (W)				
	Reactive power (Var)				
	Volt-ampere (VA)				
	Power factor (PF)				
	Frequency (Hz) Electric energy (Wh)				
4) Waveform recorder					
a) Sampling speed	1M/s				
b) Recording device	Memory record and USB reading				
c) Time accuracy	+ 500ppm				
5) AC load					
a) Resistive load	Maximum voltage: 300Vrms				
	Current range: 0 – 100A				
	Capacity: 100KW				
b) Inductive load	Maximum voltage: 300Vrms				
	Current range: 0 – 100A				
	Capacity: 100KVA				
c) Capacitive load	Maximum voltage: 300Vrms				
	Current range: 0 – 100A				
	Capacity: 100KVA				



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IEC 62116:2014 (50Hz)

3 MEASUREMENT UNCERTAINTY

Voltage measurement uncertainty	±1.5 %
Current measurement uncertainty	±2.0 %
Frequency measurement uncertainty	±0.2 %
Time measurement uncertainty	±0.2 %
Power measurement uncertainty	±2.5 %
Phase Angle	±1°
cosφ	±0.01

Note1: Measurements uncertainties showed in this table are maximum allowable uncertainties. The measurement uncertainties associated with other parameters measured during the tests are in the laboratory at disposal of the solicitant.

Note2: Where the standard requires lower uncertainties that those in this table. Most restrictive uncertainty has been considered.

4 MEASUREMENT OF AC SOURCE USED FOR TEST

Items	Desired	Measured	Deviation	Limited
Voltage(V)	230	229.9	0.04%	±2%
Voltage THD (%)	<2.5%	0.03%		<2.5%
Frequency	50	50	0.0Hz	±0.1Hz
Phase angle	120°			± 1.5°
distance	120			± 1.5



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IEC 62116:2014 (50Hz)

AC source measurement result.

change	Mode ítems		er:= = =	-	Int	ate:500mseo eg:Reset		Yokogawa 🜩
PLL	U1	Or.	U1 [V]	hdf[%]	Or.	U1 [V]	hdf[%]	_ Element1 _
Freq	50.000 Hz		229.937		dc ·			[U1 600∀rms
		1	229.944	100.000	2	0.029	0.013	I1 30Arms
Urms1	229.937 V	3	0.021	0.009	4	0.028	0.012	
Irms1	0.3661 A	5	0.037	0.016		0.022	0.010	_ Element2 _
P1	-0.0116kW	7	0.025	0.011	8	0.010	0.005	U2 600Vrms
S1	0.0842kVA	9	0.008	0.003		0.005	0.002	12 30Arms
Q1	0.0834kvar	11	0.007	0.003		0.003	0.001	
	-0.13723	13	0.007	0.003		0.004	0.002	Element3
	97.888°	15	0.006	0.002		0.001	0.000	U3 600Vrms
Uthd1 Ithd1	0.033 %	17	0.002	0.001		0.001	0.000	I3 30Arms
Pthd1	25.176 × 0.007 ×	19 21	0.004 0.007	0.002 0.003		0.006 0.003	0.003 0.001	Element4
Uthf1	0.023 ×	23	0.007	0.003		0.003	0.001	U4 600Vrms
Ithf1	3.823 %	25	0.003	0.002		0.007	0.003	I4 30Arms
Utif1	1.082	27	0.005	0.003		0.005	0.003	14 JUATINS
Itif1	164.949	29	0.003	0.003		0.006	0.003	Integ:Reset
10111	.01.010	31	0.003	0.004		0.003	0.003	
		33	0.005	0.004		0.002	0.001	:::
		35	0.006	0.003		0.002	0.001	Timer
		37	0.004	0.002		0.005	0.002	0:03:00
		39	0.004	0.002		0.003	0.001	
≏PAGE⊽ Update	7 1∕7 192				2	₽₽40 019/06/11_1	6E▼ 1⁄3	
								•
Normal	Mode		er:= = =	:		ate:500msec eg:Reset	: Eamp	Yokogawa 🔶
change	items		er:= = =	:		eg:Reset		
change PLL	items U1		er:= = = U1 [V]	■ ■ hdf[%]	Int Or.		EAMP	_ Element1 _
change	items	Iove Or.	U1 [V] 229.937		Int Or dc	eg:Reset U1 [V]	hdf[%]	Element1 U1 600Vrms
change PLL Freq	items U1 50.000 Hz	Iove Or. 41	er∶■ ■ ■ <u>U1 [V]</u> 229.937 0.003	0.001	Int Or dc 42	eg:Reset <u>U1 [v]</u> 	hdf[%] 	_ Element1 _
change PLL Freq Urms1	items U1 50.000 Hz 229.937 V	I ove Or . 41 43	U1 [V] 229.937 0.003 0.002	0.001 0.001	Int Or dc 42 44	eg:Reset <u>U1 [V]</u> 	hdf[%] 0.001 0.001	Element1 U1 600Vrms I1 30Arms
change PLL Freq Urms1 Irms1	items U1 50.000 Hz 229.937 V 0.3661 A	I ove Or. 41 43 45	U1 [V] 229.937 0.003 0.002 0.001	0.001 0.001 0.001	Int Or dc 42 44 46	eg:Reset <u>U1 [V]</u> 0.002 0.003 0.004	hdf[%] 0.001 0.001 0.002	Element1 U1 600Vrms I1 30Arms Element2
change PLL Freq Urms1 Irms1 P1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW	I ove Or . 41 43 45 47	U1 [V] 229.937 0.003 0.002 0.001 0.004	0.001 0.001 0.001 0.002	Int dc 42 44 46 48	eg:Reset <u>U1 [V]</u> 0.002 0.003 0.004 0.005	hdf[%] 0.001 0.001 0.002 0.002 0.002	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms
change PLL Freq Urms1 Irms1 P1 S1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA	I ove Or. 41 43 45 47 49	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005	0.001 0.001 0.001 0.002 0.002	Int dc 42 44 46 48 50	eg:Reset U1 [v] 0.002 0.003 0.004 0.005 0.003	hdf[%] 0.001 0.001 0.002 0.002 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2
change PLL Freq Urms1 Irms1 P1 S1 Q1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kvar	I ove Or . 41 43 45 47 49 51	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008	0.001 0.001 0.001 0.002 0.002 0.002 0.004	Int dc 42 44 46 48 50 52	eg:Reset U1 [v] 0.002 0.003 0.004 0.005 0.003 0.006	hdf[%] 0.001 0.001 0.002 0.002 0.002 0.001 0.003	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms
change PLL Freq Urms1 Irms1 P1 S1 Q1 À1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kVar -0.13723	I ove 0r. 41 43 45 47 49 51 53	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003	0.001 0.001 0.001 0.002 0.002 0.002 0.004 0.004	Int dc 42 44 46 48 50 52 52 54	eg:Reset <u>U1 [V]</u> 0.002 0.003 0.004 0.005 0.003 0.006 0.004	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.003 0.002	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3
change PLL Freq Urms1 Irms1 P1 S1 Q1 λ1 G1 G1 G1 G1 G1 G1 G1 G1 G1 G1 G1 G1 G1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kVar -0.13723 97.888 °	I ove 0r. 41 43 45 47 49 51 53 55	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003	0.001 0.001 0.002 0.002 0.002 0.004 0.004 0.001 0.001	Int dc 42 44 46 48 50 52 54 56	eg:Reset <u>U1 [V]</u> 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.004 0.003	hdf[%] 0.001 0.002 0.002 0.001 0.003 0.003 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms
change PLL Freq Urms1 Irms1 P1 S1 Q1 λ1 Φ1 G Uthd1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kVar -0.13723 97.888 ° 0.033 %	I ove 0r. 41 43 45 47 49 51 53 55 57	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003 0.002	0.001 0.001 0.002 0.002 0.002 0.004 0.004 0.001 0.001 0.001	Int dc 42 44 46 48 50 52 54 56 58	eg:Reset U1 [V] 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.003 0.005	hdf[%] 0.001 0.002 0.002 0.002 0.003 0.003 0.002 0.001 0.002	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3
change PLL Freq Urms1 Irms1 P1 S1 Q1 Q1 λ1 G Uthd1 Ithd1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kvar -0.13723 97.888 ° 0.033 % 25.176 %	I ove 0r. 41 43 45 47 49 51 53 55 57 59	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003 0.002 0.002	0.001 0.001 0.002 0.002 0.002 0.004 0.001 0.001 0.001 0.001 0.001	Int dc 42 44 46 48 50 52 54 56 58 60	eg:Reset U1 [V] 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.004 0.004 0.003 0.005 0.003	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms
change PLL Freq Urms1 Irms1 P1 S1 Q1 λ1 Φ1 G Uthd1 Ithd1 Pthd1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kvar -0.13723 97.888 ° 0.033 % 25.176 % 0.007 %	I ove 0r. 41 43 45 47 49 51 53 55 57 59 61	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003 0.003 0.002 0.002	0.001 0.001 0.002 0.002 0.004 0.004 0.001 0.001 0.001 0.001	Int dc 42 44 46 48 50 52 54 56 58 60 62	eg:Reset U1 [V] 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.003 0.005	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms Element4
change PLL Freq Urms1 Irms1 P1 S1 Q1 λ1 Φ1 G Uthd1 Ithd1 Pthd1 Uthf1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kvar -0.13723 97.888 ° 0.033 % 25.176 % 0.007 % 0.007 % 0.023 %	I ove 41 43 45 47 49 51 53 55 57 59 61 63	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003 0.002 0.002 0.002	0.001 0.001 0.002 0.002 0.002 0.004 0.001 0.001 0.001 0.001	Int dc 42 44 46 48 50 52 54 56 58 60 62 64	eg:Reset <u>U1 [V]</u> 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.003 0.005 0.003 0.005 0.003	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms Element4 U4 600Vrms
change PLL Freq Urms1 Irms1 P1 S1 Q1 λ1 φ1 G Uthd1 Ithd1 Ithd1 Uthf1 Ithf1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kVar -0.13723 97.888 ° 0.033 % 25.176 % 0.007 % 0.007 % 0.023 % 3.823 %	I ove 0r. 41 43 45 47 49 51 53 55 57 59 61 63 65	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003 0.002 0.002 0.002	0.001 0.001 0.002 0.002 0.004 0.004 0.001 0.001 0.001 0.001	Int dc 42 44 46 48 50 52 54 56 58 60 62 64 66	eg:Reset <u>U1 [V]</u> 0.002 0.003 0.004 0.005 0.003 0.004 0.004 0.003 0.005 0.003 0.005 0.003	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms Element4
change PLL Freq Urms1 Irms1 P1 S1 Q1 λ1 Φ1 G Uthd1 Ithd1 Pthd1 Uthf1 Ithf1 Utif1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0834kvar -0.13723 97.888 ° 0.033 % 25.176 % 0.007 % 0.023 % 3.823 % 1.082	Iove 41 43 45 47 51 53 55 57 59 61 63 67	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003 0.002 0.002 0.002	0.001 0.001 0.002 0.002 0.002 0.004 0.001 0.001 0.001 0.001	Int Or. 42 44 46 48 50 52 54 55 58 60 62 64 66 68	eg:Reset U1 [V] 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.003 0.005 0.003 0.005 0.003	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms Element4 U4 600Vrms I4 30Arms
change PLL Freq Urms1 Irms1 P1 S1 Q1 λ1 φ1 G Uthd1 Ithd1 Ithd1 Uthf1 Ithf1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kVar -0.13723 97.888 ° 0.033 % 25.176 % 0.007 % 0.007 % 0.023 % 3.823 %	Or . 41 43 45 47 49 51 53 55 57 59 61 	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.003 0.003 0.003 0.002 0.002 0.002	0.001 0.001 0.002 0.002 0.002 0.004 0.001 0.001 0.001 0.001	Int Or. dc 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70	eg:Reset U1 [V] 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.003 0.005 0.003 0.005 0.003	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms Element4 U4 600Vrms I4 30Arms Integ:Reset
change PLL Freq Urms1 Irms1 P1 S1 Q1 Δ1 Φ1 G Uthd1 Ithd1 Pthd1 Uthf1 Ithf1 Utif1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0834kvar -0.13723 97.888 ° 0.033 % 25.176 % 0.007 % 0.023 % 3.823 % 1.082	Iove 41 43 45 47 53 55 57 59 61 63 67 69 71	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003 0.002 0.002 0.002	0.001 0.001 0.002 0.002 0.004 0.001 0.001 0.001 0.001	Int Or. dc 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72	eg:Reset U1 [¥] 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.003 0.005 0.003 0.005 0.003 0.005 0.003	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms Element4 U4 600Vrms I4 30Arms
change PLL Freq Urms1 Irms1 P1 S1 Q1 λ1 Φ1 G Uthd1 Ithd1 Pthd1 Uthf1 Ithf1 Utif1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0834kvar -0.13723 97.888 ° 0.033 % 25.176 % 0.007 % 0.023 % 3.823 % 1.082	Iove 41 43 45 47 53 55 57 59 61 63 67 69 71	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.003 0.003 0.003 0.002 0.002 0.002	0.001 0.001 0.002 0.002 0.004 0.001 0.001 0.001 0.001	Int Or. dc 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72	eg:Reset U1 [V] 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.003 0.005 0.003 0.005 0.003	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms Element4 U4 600Vrms I4 30Arms Integ:Reset Time :-::
change PLL Freq Urms1 Irms1 P1 S1 Q1 λ1 Φ1 G Uthd1 Ithd1 Pthd1 Uthf1 Ithf1 Utif1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0834kvar -0.13723 97.888 ° 0.033 % 25.176 % 0.007 % 0.023 % 3.823 % 1.082	Iove 41 43 45 47 53 55 57 59 61 63 67 69 71	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003 0.002 0.002 0.002	0.001 0.001 0.002 0.002 0.004 0.001 0.001 0.001 0.001	Int Or. dc 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72 74	eg:Reset U1 [¥] 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.003 0.005 0.003 0.005 0.003 0.005 0.003	hdf[%] 0.001 0.002 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms Element4 U4 600Vrms I4 30Arms Integ:Reset Time : Timer
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change PLL Freq Urms1 P1 S1 Q1 λ1 G Uthd1 Ithd1 Pthd1 Uthf1 Uthf1 Utif1 Itif1	items U1 50.000 Hz 229.937 V 0.3661 A -0.0116kW 0.0842kVA 0.0834kVar -0.13723 97.888 ° 0.033 % 25.176 % 0.007 % 0.023 % 3.823 % 1.082 164.949	Iove 41 43 45 47 51 53 55 57 59 61 63 67 69 71 73 75	U1 [V] 229.937 0.003 0.002 0.001 0.004 0.005 0.008 0.003 0.003 0.002 0.002 0.002	0.001 0.001 0.002 0.002 0.004 0.001 0.001 0.001 0.001	Int Or. dc 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72 74 76 78	eg:Reset U1 [V] 0.002 0.003 0.004 0.005 0.003 0.006 0.004 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.004 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.003 0.005 0.005 0.003 0.005 0.005 0.003 0.005	hdf[%] 0.001 0.002 0.002 0.001 0.003 0.002 0.001 0.002 0.001 0.002 0.001	Element1 U1 600Vrms I1 30Arms Element2 U2 600Vrms I2 30Arms Element3 U3 600Vrms I3 30Arms Element4 U4 600Vrms I4 30Arms Integ:Reset Time : Timer
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